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Set	Items	Description
S1	15390832	S (MEMORY OR MEMORIES OR RAM OR (RANDOM(1W)ACCESS(1W)MEMORY) OR EEPROM? ? OR READ(1N)WRITE OR DRAM? ? OR SDRAM? ? OR RDRAM? ? OR DIMM? ? OR SODIMM? ? OR ECC OR PRAM OR SIMM OR DATA()STORE OR DATA()STORAGE OR STORAGE OR READ()ONLY OR CACHE()STORAGE OR BUFFER OR HD OR HARD()DRIVE OR AREA OR LOCATION OR STORAGE OR COMPACTFLASH OR SMARTMEDIA OR MEMORY()STICK OR SD()MEMORY OR XD()PICTURE OR CARD OR USB()KEY OR STORAGE OR STORE OR CACHE OR EPROM? ? OR BUFFER? ? OR DISC? ? OR DISK? ?)
S2	22432	S S1(5N)((SECOND OR 2ND OR TWO OR 2 OR MULTIPLE OR TWOFOLD OR DUAL OR PLURAL OR PLURALITY OR MULTIPLE? OR MULTI OR PAIR??)(2N)BUFFER? ?) OR GPU OR (GRAPHIC? ?(1W)PROCESS?(1W)UNIT? ?) OR COPROCESSOR? ? OR (COPROCESSOR? ?)(READABLE))
S3	144	S S2(10N)(PAGING OR MAPP???)
S4	20972	S S1(5N)((PROPER OR CORRECT OR RIGHT OR MEET DECOROUS OR DISCREET? ? OR BELONG? FIT OR FITTING)(3N)(LOCATION? ? OR ADDRESS? ? OR SPACES? ? OR POSITION? ? OR REGION? ?))
S5	106457	S S1(5N)(INDICATOR? OR POINTER? ? OR INDEX? OR GAUGE OR BELLWETHER? ? OR DETECTOR? ?)

S6 144 S S3(100N)S2  
S7 0 S S6(100N)S4  
S8 4 S S6(100N)S5

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## Subject summary

? t /3,k/all

8/3,K/1 (Item 1 from file: 148) [Links](#)

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11587200 Supplier Number: 55587411 (USE FORMAT 7 OR 9 FOR FULL TEXT )

TEXAS INSTRUMENTS TMS320C5X.(Product Announcement)

Levy, Markus

EDN , 44 , 8 , 87

April 15 , 1999

Document Type: Product Announcement

ISSN: 0012-7515

Language: English

Record Type: Fulltext

Word Count: 682 Line Count: 00056

...direct addressing, in which 7 bits in instruction concatenate with a 9-bit data-page pointer for accessing data RAM (128 words each page). It also supports indirect, immediate, dedicated-register, and memory-mapped-register addressing. The processor supports automatic circular-buffer addressing for two buffers. The addressing mechanism supports buffer wraparound if the address-generation unit steps on the end of the buffer but not...

8/3,K/2 (Item 2 from file: 148) [Links](#)

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10218796 Supplier Number: 20579572 (USE FORMAT 7 OR 9 FOR FULL TEXT )

Texas Instruments TMS320C5x.(digital signal processor)

EDN , v43 , n9 , p74(1)

April 23 , 1998

ISSN: 0012-7515

Language: English

Record Type: Fulltext; Abstract

Word Count: 672 Line Count: 00056

...direct addressing, in which 7 bits in instruction concatenate with a 9-bit data-page pointer for accessing data RAM (128 words each page). It also supports indirect, immediate, dedicated-register, and memory-mapped-register addressing. The processor supports automatic circular-buffer addressing for two buffers. The addressing mechanism supports buffer wraparound if the address-generation unit steps on the end of the buffer but not...

8/3,K/3 (Item 3 from file: 148) [Links](#)

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09644395 Supplier Number: 16956403 (USE FORMAT 7 OR 9 FOR FULL TEXT )

EDN's 1995 DSP-chip directory. (general-purpose digital signal processing chips)(Directory)

Levy, Markus; Leonard, James P.

EDN , v40 , n10 , p40(25)

May 11 , 1995

Document Type: Directory

ISSN: 0012-7515

Language: English

Record Type: Fulltext; Abstract

Word Count: 16708 Line Count: 01317

...modes -- Paged memory direct addressing: 7 bits in instruction concatenate with 9-bit data-page pointer for accessing data RAM (128 words each page), indirect, immediate, dedicated register, memory-mapped register. The processor supports automatic circular buffer addressing for two buffers; however, this addressing mechanism lacks wrap-around capability on overshoot.

Special instructions -- Single and block...

8/3,K/4 (Item 4 from file: 148) [Links](#)

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08928018 Supplier Number: 18540527 (USE FORMAT 7 OR 9 FOR FULL TEXT )

16-bit.(EDN DSP Directory)

EDN , v41 , n5 , p51(14)

March 1 , 1996

ISSN: 0012-7515

Language: English

Record Type: Fulltext; Abstract

Word Count: 13459 Line Count: 01062

...modes - Paged-memory direct addressing: 7 bits in instruction concatenate with 9-bit data-page pointer for accessing data RAM (128 words each page), indirect, immediate, dedicated register, memory-mapped register. The processor supports automatic circular buffer addressing for two buffers; however, this addressing mechanism lacks wraparound capability on overshoot.

Special instructions - Single and block repeat...

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